RRAM in IoT

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IoT In the Next Few Years

Internet Connection Demands Increasing

3B PCs, tablets and smartphones today

IoT nodes increasing from:

9B in 2013 ▶ **28B** by 2020

Computation Increasingly Moving to Nodes

Technology Drivers Supporting Node Deployment

- Sensors becoming increasingly affordable
- Bandwidth cost dropped by 40x in the last 10 years
- Processing costs dropped 60x in the last 10 years
- Smartphones as a gateway for IoT nodes over the internet

RRAM as NVM Alternative in IoT

Data Center – Block Oriented Data Storage

- Low latency(10^{-5} s), high bandwidth, low energy
- Native 3D compatible array architecture
- Alternatives: SSD, DRAM (disk cache), hard disk

Nodes – XiP Code and Random Access Data

- Low latency (10^{-8} s), high bandwidth, low energy
- CMOS BEOL compatible
- Alternatives: embedded NOR, discrete NOR

Existing NV Memory Technology Comparison

Feature	Incumbent NVM		RRAM	
	Embedded NOR	NAND	Embedded 1T1R	1TnR
Random Read Time	25ns – 35ns	25us - 75us	30ns	0.5us - 1us
Program Time	268us/128B	>1000us /8KB (MLC)	12us/4B	64us/8KB
Endurance	10^5	MLC 10^3	10^5	10^8 - 10^{12}
Cell Size	0.09um^2@40nm	SLC 5F^2 MLC	0.1um^2@40nm	SLC 4F^2, Stacking, MLC
Erase Time/Size	168ms/16KB	>2ms(Block)	**Erase Not Required EEPROM Emulation!**	
Cost	Med	Low	Low	Very Low

Crossbar's RRAM-based Technology

Simple, 3 Layer Cell Structure

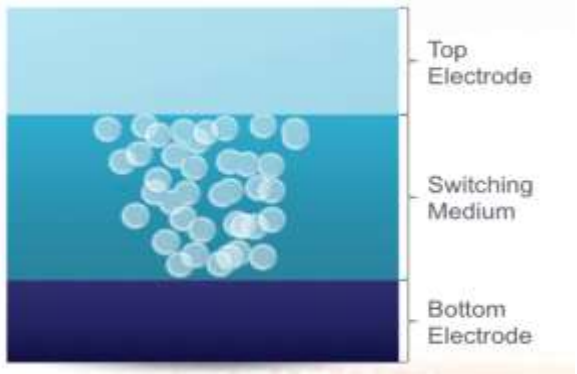
- Metallic top electrode
- Resistive switching medium
- Non-metallic bottom electrode
- Electric field based filamentary switching

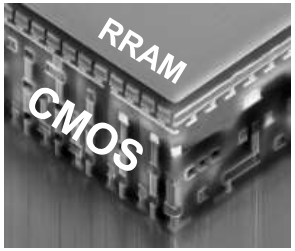
CMOS Back-End-Of-Line Compatible

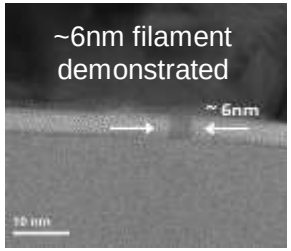
- RRAM layer(s) on top of CMOS logic
- Filament sizes less than 10nm demonstrated
- On/Off ratio improves with smaller geometries

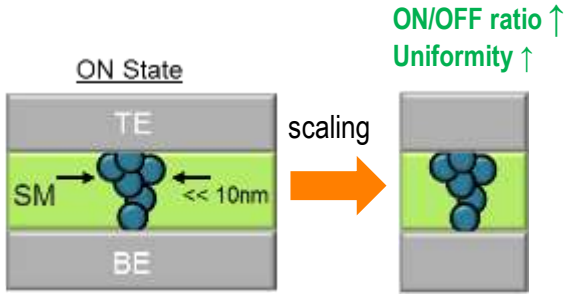
Array Architectures

- Code storage (1T1R)
  - Low latency
- Data storage (1TnR)
  - Approaching $4F^2$ memory cell for data storage
  - Natively 3D stackable









Crossbar Development Efforts

1T1R Embedded RRAM Macro → **1TnR Discrete Device**

- 2Mb to 64Mb densities
- Hard macro using 40nm logic

- RRAM in IoT Chipsets
  - Scale to smaller geometries
  - Simple NVM process integration
  - Higher performance
  - Code and high-density data storage on same chip

Thank You